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10/632,154	07/30/2003	Yi Ding	M-15230 US	1878

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,154	YI DING	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 30-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 30-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/09/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The Information Disclosure Statement filed on November 09th, 2004 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-17 and 30-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Yaegashi et al. (U.S. Patent 6,265,739).

In re claim 1, **Yaegashi** discloses a method for fabricating an integrated circuit comprising a nonvolatile memory comprising a nonvolatile memory cell comprising two floating gates (**106**, in MEMORY CELL region), a select gate (inside the SELECT TRANSISTOR), and two control gates (**107**, in MEMORY CELL region), the nonvolatile memory further comprising a first peripheral transistor (**Vpp-Tr**), the method comprising: (a) forming a dielectric layer on a semiconductor substrate **101**, the dielectric layer comprising a first dielectric region **108** ("select gate dielectric'') and a second dielectric region (**108**, inside Vpp-Tr) ("first peripheral transistor gate dielectric'') (col. 7, line 57 to col. 8, line 29), wherein the select gate dielectric and the first peripheral transistor gate dielectric are formed simultaneously (col. 9, lines 53-61); (b) forming a first layer over the dielectric layer and patterning the first layer to provide (i) the select

gate on the select gate dielectric **(SELECT TRANSISTOR)**, and (ii) a gate for the first peripheral transistor on the first peripheral transistor gate dielectric **(Vpp-Tr)** (col. 8, lines 41-54); (c) after forming the first layer, forming one or more second layers which provide the floating gates **(106, in MEMORY CELL region)** and the control gates **(106, in MEMORY CELL region)** for the memory cell (FIGS. 1-4B).

In re claim 2, **Yaegashi** discloses wherein the memory cell comprises a continuous channel region in the semiconductor substrate **101**, the select gate controls a conductivity of a portion of the channel region, and each of the floating gates **106** overlies a respective other portion of the channel region (col. 10, lines 16-65 and **FIGS. 4A-6C**).

In re claim 3, **Yaegashi** discloses wherein the control gates **107** overlie the respective floating gates **106 (FIG. 4A)**.

In re claim 4, **Yaegashi** discloses wherein the one or more second layers are a plurality of layers (**106** and **107**).

In re claim 5, **Yaegashi** discloses wherein the select gate dielectric **108** and the first peripheral transistor gate dielectric **108** (in Vpp-Tr region) are formed by oxidation of the semiconductor substrate **101** (FIG. 4A) (col. 9, lines 32-34).

In re claim 6, **Yaegashi** discloses wherein the select gate dielectric **108** and the first peripheral transistor gate dielectric **108** (in Vpp-Tr region) comprise silicon oxide (col. 9, lines 22-34).

In re claim 7, **Yaegashi** discloses wherein the method of Claim 1 further comprising, after forming the first layer, forming a dielectric **105** ("floating gate

dielectric") on the semiconductor substrate **101** to separate the floating gates **106** from the substrate, wherein the floating gate dielectric (8nm thick) is formed of the same material as the select gate dielectric **108** (40 nm thick) (col. 9, lines 53-61) but is thinner than the select gate dielectric (col. 8, lines 30-39 and **FIG. 4A**).

In re claim 8, **Yaegashi** discloses wherein the method of Claim 1 further comprising forming a second peripheral transistor gate dielectric **118** (Vcc-Tr) on the semiconductor substrate **101** for a second peripheral transistor (Vcc-Tr), and forming a gate **106, 107** of the second peripheral transistor on the second peripheral transistor gate dielectric, wherein the second peripheral transistor gate dielectric **118** is made from the same material as the select gate dielectric **108** (SELECT TRANSISTOR) and the first peripheral transistor gate dielectric **108** (Vpp-Tr) but the thickness of the second peripheral transistor gate dielectric (8 nm thick) is different from the thickness of the first peripheral transistor gate dielectric (40 nm) (col. 9, lines 53-61 and **FIG. 4A**).

In re claim 9, **Yaegashi** discloses wherein the second peripheral transistor gate dielectric **118** (Vcc-Tr) (8nm thick) is thinner than the first peripheral transistor gate dielectric **108** (Vpp-Tr) (40nm thick) (col. 9, lines 53-61 and **FIG. 4A**).

In re claim 10, **Yaegashi** discloses wherein the select gate dielectric as at least as thick as a gate dielectric of any peripheral transistor in the memory (col. 9, lines 53-61 and **FIG. 4A**).

In re claim 11, **Yaegashi** discloses wherein the second peripheral transistor gate dielectric is formed after the start of the operation (a) (col. 9, lines 16-61 and **FIGS. 1-4A**).

In re claim 12, **Yaegashi** discloses wherein the second peripheral transistor gate dielectric **118** (Vcc-Tr) is formed before the operation (b) (col. 9, lines 53-61 and FIGS. 1-4A).

In re claim 13, **Yaegashi** discloses wherein the gate **106** and **107** of the second peripheral transistor (Vcc-Tr) is formed by patterning the first layer in the operation (b) (col. 8, lines 5-54 and **FIGS. 1-4A**).

In re claim 14, **Yaegashi** discloses wherein the memory cell is one of a plurality of nonvolatile memory cells of the memory, each memory cell comprising two floating gates **106**, a select gate (in SELECT TRANSISSTOR), and two control gates **107**, wherein: the operation (a) simultaneously forms select gate dielectric for each of the memory cells; and the operation (b) simultaneously forms the select gate for each of the memory cells on the corresponding select gate dielectric (col. 8, lines 5-54 and **FIGS. 1-4A**).

In re claim 15, **Yaegashi** discloses wherein during a memory cell writing operation, the first peripheral transistor (Vpp Tr) is exposed to a voltage of a higher magnitude than any voltage provided to the memory cell in a reading operation (col. 7, line 57 to col. 8, line 4 and **FIGS. 1-4A**).

In re claim 16, **Yaegashi** discloses wherein during the memory cell writing operation, the first peripheral transistor is exposed to a voltage of a higher magnitude than any power supply voltage provided to the nonvolatile memory (col. 7, line 57 to col. 8, line 4 and **FIGS. 1-4A**).

In re claim 17, **Yaegashi** discloses wherein the memory is to support a writing operation in which the memory cell is written by a transfer of a charge between one of the floating gates and a channel region of the memory cell, the channel region being located in the semiconductor substrate (col. 7, line 57 to col. 8, line 39 and **FIGS. 1-4A**).

In re claim 30, **Yaegashi** discloses that the operation (c) further comprises patterning the one or more second layers to provide the floating and control gates (FIG. 4A).

In re claim 31, **Yaegashi** discloses that the first layer patterning comprises:

(b1) patterning the first layer to provide the select gate; and

(b2) patterning the first layer to provide the gate for the first peripheral transistor;

wherein the operation (c) is performed after the operation (b1) but before the operation (b2) (col. 8, lines 5-54 and FIG. 4A).

In re claim 32, **Yaegashi** discloses that the method of Claim 1 further comprising, after forming the first layer but before forming the one or more second layers, forming a dielectric ("floating gate dielectric") on the semiconductor substrate to separate the floating gates from the substrates (col. 8, lines 5-54 and FIG. 4A).

In re claim 33, **Yaegashi** discloses wherein the first layer patterning comprises:

(b1) patterning the first layer to provide the select gate; and

(b2) patterning the first layer to provide the gate for the first peripheral transistor;

wherein the floating gate dielectric is formed after the operation (b1) (col. 8, lines 5-54 and FIG. 4A).

In re claim 34, **Yaegashi** discloses that the memory cell comprises a continuous channel region in the semiconductor substrate, and each of the floating gates controls a conductivity of a respective portion of the channel region (col. 8, lines 5-54 and FIG. 4A).

In re claim 35, **Yaegashi** discloses that the select gate controls the conductivity of a portion of the channel region (col. 8, lines 5-54 and FIG. 4A).

In re claim 36, **Yaegashi** discloses that the channel's portion whose conductivity is controlled by the select gate is between the channel's portions whose conductivities are controlled by the floating gates (col. 8, lines 5-54 and FIG. 4A).

In re claim 37, **Yaegashi** discloses that the memory cell comprises two source/drain regions and a continuous channel region bordering on the source/drain regions, and each floating gate of the memory cell overlies a portion of the channel region (col. 8, lines 5-54 and FIG. 4A).

In re claim 38, **Yaegashi** discloses that the floating gates are adjacent to respective two opposite sidewalls of the select gate and are insulated from the select gate (col. 8, lines 5-54 and FIG. 4A).

Response to Applicant's Amendment and Arguments

Applicant's arguments filed October 26th, 2004 have been fully considered but they are not persuasive.

Applicant contends that Yaegashi does not teach or suggest forming the floating gate layer after the select or peripheral transistor gate layer.

In response to Applicant's contention that Yaegashi does not teach or suggest forming the floating gate layer after the select or peripheral transistor gate layer, Examiner respectfully disagrees. It is noted that the features upon which applicant relies (i.e., forming the floating gate layer after the select or peripheral transistor gate layer) are not explicitly recited in the rejected claim(s) since Applicant's claimed invention has a layer and a layer can be at any location. Thus, Applicant's first layer does not preclude the Examiner from the use of the Yaegashi reference. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

For these reasons, examiner holds the rejection proper.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
January 3rd, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER